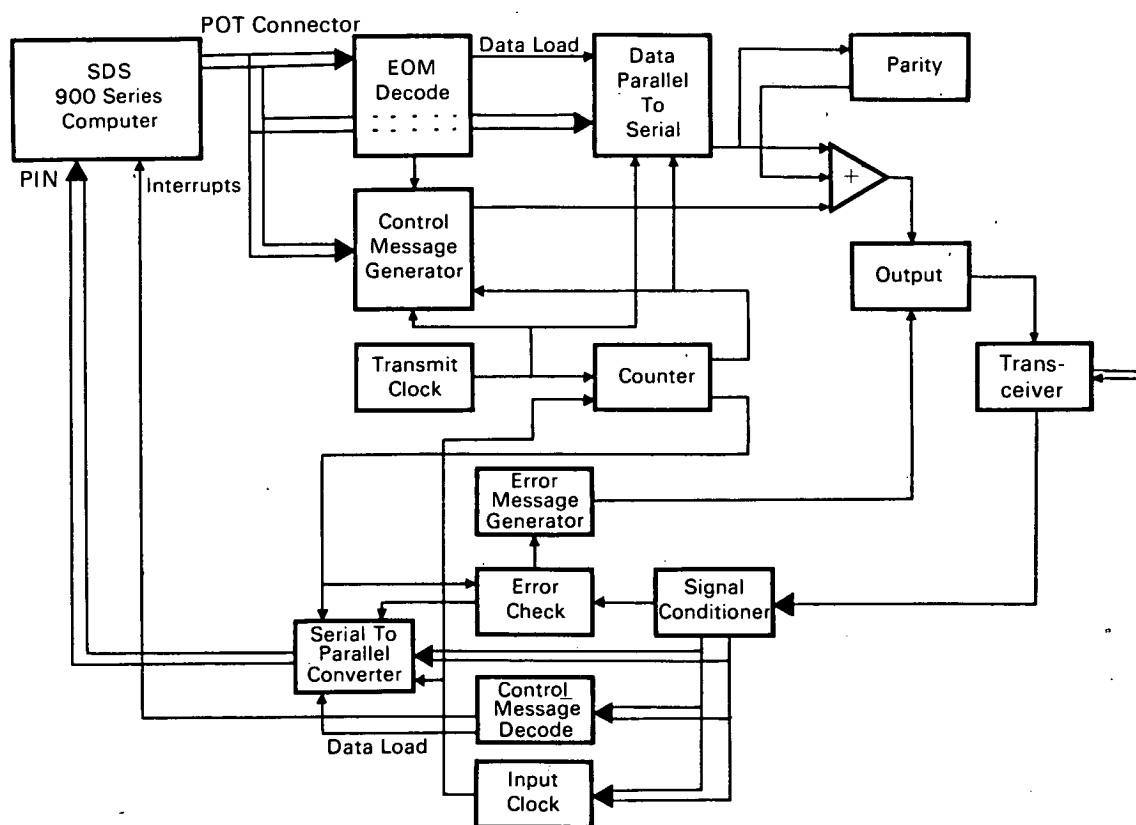


NASA TECH BRIEF



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Communications Link for SDS 900 Series Computers



The problem:

To design a combined system of two or more computers with a minimum number of connections in order to reduce data errors substantially.

The solution:

Develop a high speed, self-clocking single channel control and data link apparatus to interface between the two computers.

How it's done:

The block diagram above depicts the interfacing circuitry associated with the computer at one end of the communications link. Identical circuitry is associated with the computer at the other end of the link.

The transmitted output from the remote computer is received in serial form by the transceiver shown

(continued overleaf)

at the far right in the diagram. Timing circuits determine if a complete data and control message has been received, and check the composite signal for correct parity and rate. If errors are present, an error control message is sent back to the originating computer. If the signal is normal, it is converted from series to parallel form and input to the local computer (PIN), which then acts on the control and data components to perform the task programmed.

To transmit, the data in parallel output form (POT) is fed through the energize output medium (EOM) decode to the parallel-to-serial converter. The EOM senses the start of a transmission and activates the appropriate equipment to route the data to the transceiver. The serial data, together with control codes and a parity bit, are fed to the output driver which converts the pulses to a three-level form (+5 volts for the 1 state; -5 volts for the 0). Transmission of the data in this form removes the necessity of transmitting a clock signal on a separate channel.

Note:

Requests for further information may be directed to:

Technology Utilization Officer
NASA Pasadena Office
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Patent status:

No patent action is contemplated by NASA.

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